Cont C1

connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit.

C2

8. (Amended) The semiconductor integrated circuit device as claimed in Claim 1, wherein the input signal (VIN) is realized by a word line selecting signal; the driver circuit is realized by a word line driver; the first long-distance wiring is realized by a word line (WL); and the gate circuits are realized by memory cells.

9. (Amended) The semiconductor integrated circuit device as claimed in Claim 1, wherein the input signal (VIN) is realized by a clock input signal (VCK); the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.

C3

10. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-

increasing circuit, wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second long-distance wiring.

11. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.

12. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-

increasing circuit, wherein a plurality of speed-increasing circuits are additionally inserted between an intermediate position of the second long-distance wiring and the vicinity of the input terminal of the gate circuit connected to a position corresponding to the intermediate position.

13. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a plurality of buffer circuits are inserted at the input side of the second long-distance wiring.

14. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit

connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a buffer circuit is inserted at the input side of the second long-distance wiring, and a buffer circuit is inserted at the output side of the second long-distance wiring.

15. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the input signal (VIN) is realized by a clock input signal (VCK); the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.